REMARKS

The Examiner has finally rejected claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,157,492 to Tults in view of U.S. Patent 4,405,947 to Tults et al.

The Tults patent discloses sync validity detecting utilizing a microcomputer, which includes a phase-locked loop 115 connected between a tuner 101 and a microcomputer 117 for tuning the tuner to a desired signal, and an AFT circuit (AFT detector 109 and AFT comparators 127) connected between an output of the tuner 101 and the microcomputer 117.

The Tults et al. patent discloses a dual search mode type tuning system in which a phase-locked loop is first used followed by operation of an AFT circuit.

Claim 1 (and claim 7) include the limitations "...a stage for receiving tuned signals from said tuner and for supplying at least one control signal to said controller, wherein said stage comprises an automatic fine tuning unit for generating an automatic fine tuning signal and a phase-locked-loop for generating a lock signal more quickly available than the automatic fine tuning signal, said lock signal forming said at least one control signal for said controller to provide an indication whether a channel at a tuned frequency is active or not."

The Examiner has indicated that Tults teaches:

> "c) the claimed a stage for receiving tuned signals.. .is met by PLL 115, AFT (detector 109, 127), video detector 105/Sync Separator III which receive tuning signals (signals from the tuner). The stage being the components not included in the tuner or microcomputer.

> PLL 115 along with AFT circuitry (127/109) and Sync separator III provide input into the controller (microcomputer 117). It is noted that the PLL III is connected to the controller (microcomputer 117) via input/output terminals 121 and 119 (Fig 1), wherein AFT comparators 127 provides the indication of a carrier signal to controller 117, in addition a sync separator III provides the validation whether a horizontal sync has been detected, to affirm a picture carrier not sound carrier has been detected. The control signals (both AFT and Sync Ill) originate from the PLL in order to lock onto to the appropriate frequency/phase."

Applicants submit that while the PPL 115 of Tults receives "tuning signal", the PPL 115 is not part of a stage that receives "tuned signals" as specifically stated in, for example, claim 1. In particular, a tuner receives an antenna signal and a tuner signal from which it generates an oscillator signal for mixing with the antenna signal in order to output desired tuned signals. In Tults, the tuned signals are applied, via an IF stage 103 to a video detector 105 and the AFT detector 109. In contrast therewith, the PLL 115 does not received the tuned signal. Rather, the PLL 115 receives an "LO" signal from the tuner 101. As clearly indicated in Tults at col. 2, lines 52-57, the LO signal is a local oscillator signal from the tuner 101 which is used in the tuner for tuning to the desired signals. Hence, any lock signal from the PLL only indicates that the oscillator/tuning signal is at the chosen frequency. However, the PLL 115 and the lock signal therefrom cannot form "at least one control signal for said controller to provide an indication whether a channel at a tuned frequency is active or not."

Hence, Applicants submit that Tults does not disclose or suggest "...a stage for receiving tuned signals from said tuner and for supplying at least one control signal to said controller, wherein said stage comprises an automatic fine tuning unit for generating an automatic fine tuning signal and a phase-locked-loop for generating a lock signal more quickly available than the automatic fine tuning signal, said lock signal forming said at least one control signal for said controller to provide an indication whether a channel at a tuned frequency is active or not."

Further, claim 9 includes the steps "tuning said tuner to one of a plurality of frequencies at which video signal should be located", "determining whether a channel is active at the tuned frequency using a phase-locked-loop in said stage, said phase-locked loop generating a lock signal in response thereto in a manner more quickly available that an automatic fine tuning signal of an automatic fine tuning unit of the stage" and "controlling the tuner with a control signal comprising said lock signal".

Applicants submit that the PLL 115 of Tults is merely used in the step "tuning said tuner to one of a plurality of frequencies at which video signal should be located". However, in order to determine whether a channel is active at the tuned frequency, as with the AFT circuit, the phase-locked loop, as part of the stage, must be connected to the tuned signals, as opposed to the oscillator signal.

With regard to the Tults et al. patent, as with Tults, the phase-locked loop is connected to receive the tuning/oscillator signal. As such, Tults et al. does not supply that which is missing from Tults.

In view of the above, Applicants believe that the subject invention, as claimed, is not rendered obvious by the prior art, either individually or collectively, and as such, is patentable thereover.

Applicants believe that this application, containing claims 1-10, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

by___/Edward W. Goodman/_____
Edward W. Goodman, Reg. 28,613
Attorney
Tel.: 914-333-9611